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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,562	09/25/2003	Tetsuya Shimomura	503.35686CX3	4025

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EXAMINER	
CHAUHAN, ULKA J	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,562	SHIMOMURA ET AL.	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,8,13 and 14* is/are rejected.

7)☒ Claim(s) *3-6,9-12 and 15-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/942,689.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/5/03; 9/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 2, 7, 8, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,002,411 to Dye and U.S. Patent No. 5,818,464 to Wade.

4. As per claim 1, Dye teaches an integrated memory controller (IMC) comprising:

a CPU interface arranged to interface with a CPU (Fig. 5 and c. 16 ll. 12-18: *bus interface logic 202 for coupling to the host*);

a memory interface arranged to interface with a memory storing programs to be processed in the CPU and display data to be displayed on a display (Fig. 5 and c. 16 ll. 42-47: *memory control units 220 and 222 provide interface signals to communicate with respective banks of system memory 110*; c. 22 ll. 63-c. 23 ll. 9: *some regions are allocated as screen memory for display output, and other regions are allocated for CPU instruction execution*);

a display control circuit to control output of display data to the display (Fig. 5 and c. 17 ll. 29-32 and ll. 51-55: *information in each respective window workspace is used by the Window Assemble 240 during screen refresh to draw the respective window information on the display screen 142*);

a rendering process circuit to access the memory (Fig. 5 and c. 16 ll. 31-41: *graphics engine 212 includes polygon rendering logic*); and

a memory control circuit to control access to the memory from one of the CPU, the display controller and the rendering processor (c. 9 ll. 42-45: *the integrated memory controller 140 integrates memory controller and video and graphics controller capabilities into a single logical unit*).

Dye also discloses that IMC 140 allows for software programmable priority for different memory accesses and that in some cases it is more important to allow CPU access to have higher priority than graphics operations (c. 24 ll. 37-43). However, Dye does not expressly teach:

wherein, when an access to the memory from the CPU is requested at the time when the rendering process circuit accesses the memory, the memory control circuit stops the access to the memory from the rendering process circuit until the access to the memory from the CPU ends, and when the access to the memory from the CPU ends, resumes the access to the memory from the rendering process circuit from the beginning.

Wade discloses a method for arbitrating access requests to a shared system memory in which if the graphics controller request has a lower priority than a competing memory controller request, and the graphics controller is determined to be in control, then the arbitration unit transmits a signal to the graphics controller requesting the graphics controller to relinquish control of the memory system, step 212. The arbitration unit then waits until the graphics controller

relinquishes control then grants control to the memory controller. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Dye and Wade whereby when CPU accesses have high priority than graphics operations, the graphics operations are requested to relinquish control as taught by Wade in order to allow CPU accesses to complete and avoid system performance degradation. It would also have been obvious to one of ordinary skill in the art at the time the invention was made to have resumed graphics operations after CPU access completion in order to complete graphics operations necessary for desired graphics processing.

5. As per claim 2, Dye discloses, wherein the memory control circuit is connected to the CPU, via a CPU bus, and to the memory, via a memory bus, for providing priority to the access from the CPU to the memory (Figs. 2, 3, and 4).

6. Claims 7-8 and 13-14 are similar in scope to claims 1-2, and are rejected under the same rationale.

Allowable Subject Matter

7. Claims 3-6, 9-12, and 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the cited prior art does not disclose or render obvious the combination of elements recited in claims 3, 9, and 15, as a whole.

Conclusion

9. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is (703) 305-9651. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (703) 308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
September 14, 2004